Application No. 10/665171 (Docket: CNTR.2213)
37 CFR 1.111 Amendment dated 06/15/2006
Reply to Office Action of 02/27/2006

AMENDMENTS TO THE CLAIMS

Please cancel claims 17-31 without prejudice. Kindly amend claims 1, 17, and 32 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1.   (Currently Amended) An apparatus in a pipeline microprocessor, for ensuring coherency of instructions within stages of the pipeline microprocessor, the apparatus comprising:

   instruction cache management logic, configured to receive an address corresponding to a next instruction to be fetched, and configured to detect that a part of a memory page corresponding to said next instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within said part of said memory page and, upon detection, configured to provide said address; and

   synchronization logic, configured to receive said address from said instruction cache management logic, and configured to direct data cache management logic to check for coherency of the instructions within said part of said memory page, and, if the instructions are not coherent within said part of said memory page, said synchronization logic is configured to direct the pipeline microprocessor to stall a fetch of said next instruction to be fetched until the stages of the pipeline microprocessor have executed all preceding instructions.

2.   (Original) The apparatus as recited in claim 1, wherein said instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to said address to detect that said part cannot be freely accessed.

3.   (Original) The apparatus as recited in claim 2, wherein said ITLB entry corresponds to said memory page.

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4. (Original) The apparatus as recited in claim 3, wherein said ITLB entry comprises a plurality of part-page ownership bits.

5. (Original) The apparatus as recited in claim 4, wherein one of said plurality of part-page ownership bits corresponds to said part of said memory page.

6. (Original) The apparatus as recited in claim 5, wherein remaining ones of said plurality of part-page ownership bits correspond to remaining parts of said memory page.

7. (Original) The apparatus as recited in claim 5, wherein said part can be freely accessed if said one of said plurality of part-page ownership bits is set.

8. (Original) The apparatus as recited in claim 5, wherein said part cannot be freely accessed if said one of said plurality of part-page ownership bits is not set.

9. (Original) The apparatus as recited in claim 4, wherein said plurality of part-page ownership bits comprise four part-page ownership bits, and wherein said part comprises one-quarter of said memory page.

10. (Original) The apparatus as recited in claim 1, wherein said data cache management logic evaluates a data translation lookaside buffer (DTLB) entry corresponding to said address to detect that the instructions are not coherent within said part of said memory page.

11. (Original) The apparatus as recited in claim 10, wherein said DTLB entry corresponds to said memory page.

12. (Original) The apparatus as recited in claim 11, wherein said DTLB entry comprises a plurality of part-page ownership bits.

13. (Original) The apparatus as recited in claim 12, wherein one of said plurality of part-page ownership bits corresponds to said part of said memory page.

14. (Original) The apparatus as recited in claim 13, wherein remaining ones of said plurality of part-page ownership bits correspond to remaining parts of said memory page.

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15.   (Original) The apparatus as recited in claim 13, wherein the instructions are not coherent within said part if said one of said plurality of part-page ownership bits is set.

16.   (Original) The apparatus as recited in claim 13, wherein the instructions are coherent within said part if said one of said plurality of part-page ownership bits is not set.

17.   (Cancelled)

18.   (Cancelled)

19.   (Cancelled)

20.   (Cancelled)

21.   (Cancelled)

22.   (Cancelled)

23.   (Cancelled)

24.   (Cancelled)

25.   (Cancelled)

26.   (Cancelled)

27.   (Cancelled)

28.   (Cancelled)

29.   (Cancelled)

30.   (Cancelled)

31.   (Cancelled)

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32.   (Currently Amended) A method in a pipeline microprocessor, for ensuring coherency of instructions within stages of the pipeline microprocessor, the method comprising:

within a data cacheinstruction cache, detecting that a part of a memory page corresponding to a pending store instructionnext instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within the part of the memory page;

directing logic within an instructiona data cache to check for coherency of the instructions within the part of the memorymemory page; and

if the instructions are not coherent, flushing preceding stages of the pipeline microprocessorstalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions.

33.   (Currently Amended) The method as recited in claim 32, wherein said detecting comprises:

evaluating a data translation lookaside buffer (DTLB)an instruction translation lookaside buffer (ITLB) entry corresponding to a target an address for the pending storenext instruction.

34.   (Currently Amended) The method as recited in claim 33, wherein the DTLB entryITLB entry corresponds to the memory page.

35.   (Currently Amended) The method as recited in claim 34, wherein the DTLB entryITLB entry comprises a plurality of part-page ownership bits.

36.   (Original) The method as recited in claim 35, wherein one of the plurality of part-page ownership bits corresponds to the part of the memory page.

37.   (Original) The method as recited in claim 36, wherein remaining ones of the plurality of part-page ownership bits correspond to remaining parts of the memory page.

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38. (Original) The method as recited in claim 37, wherein the part of said memory page can be freely accessed if the one of the plurality of part-page ownership bits is set.

39. (Original) The method as recited in claim 37, wherein the part of the memory page cannot be freely accessed if the one of the plurality of part-page ownership bits is not set.

40. (Original) The method as recited in claim 35, wherein the plurality of part-page ownership bits comprise four part-page ownership bits, and wherein the part comprises one-quarter of the memory page.

41. (Currently Amended) The method as recited in claim 32, wherein said directing comprises:

evaluating ~~an instruction~~a data translation lookaside buffer ~~(ITLB) entry~~ (DTLB entry corresponding to ~~a target address~~the address for the ~~pending store~~ next instruction.

42. (Currently Amended) The method as recited in claim 41, wherein the ~~ITLB entry~~ DTLB entry corresponds to said memory page.

43. (Currently Amended) The method as recited in claim 42, wherein the ~~ITLB entry~~ DTLB entry comprises a plurality of part-page ownership bits.

44. (Original) The method as recited in claim 43, wherein one of the plurality of part-page ownership bits corresponds to the part of the memory page.

45. (Original) The method as recited in claim 44, wherein remaining ones of the plurality of part-page ownership bits correspond to remaining parts of the memory page.

46. (Original) The method as recited in claim 45, wherein the instructions are not coherent within the part if the one of said plurality of part-page ownership bits is set.